

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:

Hirotsugu KOJIMA et al.

Appln. No.:

Group Art Unit:

Filed: HERewith

For: SEMICONDUCTOR INTEGRATED CIRCUIT AND ELECTRONIC
SYSTEM

* * *

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

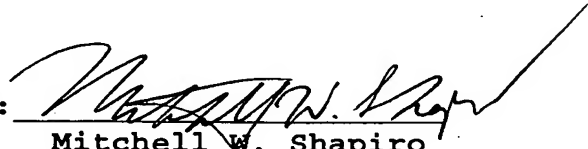
Pursuant to 37 C.F.R. § 1.56, and without any
assertion as to materiality or prior art effect, the
document listed on the attached Form PTO-1449 is hereby
cited.

The document on the attached List is cited in the
specification, on pages 3-4, and its relevance is indicated
therein.

Respectfully submitted,

MWS:lat

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By: 
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April 14, 2004

FORM PTO-1449

Atty. Docket No.

Appln. No.

XA-10077

LIST OF DOCUMENTS CITED BY APPLICANT

Applicant

Hirotsugu KOJIMA et al.

Filing Date

HEREWITH

Group

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
	AJ	10-041746	2/13/98	Japan			Abstract
	AK						
	AL						
	AM						
	AN						
	AO						

OTHER (including author, title, date, pertinent pages, etc.)

	AP	
	AQ	
	AR	

Examiner

Date Considered

XAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.